This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-2. (canceled)

3. (currently amended): ~~The method of claim 2 further~~ A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors;

after forming said off-set spacers, performing a DDD implant to form DDD source and DDD drain regions in the body region for the first transistor;

after said DDD implant, forming main spacers adjacent the off-set spacers of at least ~~the first and second transistors or of~~ the second transistor ~~only~~;

after forming said main spacers, performing a LDD implant to form LDD source and LDD drain regions for the second transistor; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

4. (original): The method of claim 3 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions is inversely dependent on a thickness of the off-set spacers,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only, and

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers.

5. (currently amended): ~~The method of claim 2 further~~ A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors;

after forming said off-set spacers, performing a DDD implant to form DDD source and DDD drain regions in the body region for the first transistor;

performing a LDD implant to form LDD source and LDD drain regions for the second transistor;

after both said DDD and LDD implants, forming main spacers adjacent the off-set spacers of the first and second transistors; and

after forming said main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and DDD source regions and each of the LDD drain and LDD source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

6. (original): The method of claim 5 wherein,

the extent of an overlap between the gate electrode of the first transistor and each of the DDD source and DDD drain regions, and the extent of an overlap

between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a thickness of the main spacers, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

7. (original): The method of claim 5 wherein N- type impurities is used in each of the DDD and LDD implants, and N+ type impurities is used in the S/D implant.

8. (original): The method of claim 5 wherein P- type impurities is used in each of the DDD and LDD implants, and P+ type impurities is used in the S/D implant.

9. (currently amended): ~~The method of claim 1 wherein said gate electrode forming act includes forming a gate electrode for each of first and second transistors, and said off-set spacers forming act includes forming off-set spacers along side-walls of the gate electrodes of the first and second transistors, said source and drain regions forming act further comprising:~~ A method of forming semiconductor transistors, comprising:

forming a gate electrode over but insulated from a semiconductor body region for each of first and second transistors;

forming off-set spacers along side-walls of the gate electrode of each of the first and second transistors; and

after forming said off-set spacers, performing a LDD implant to from LDD source and LDD drain regions in the body region for the second transistor.

10. (original): The method of claim 9 further comprising:

prior to forming the off-set spacers, performing a DDD implant to from DDD source and DDD drain regions in the body region for the first gate electrode;

after said LDD implant, forming main spacers adjacent the off-set spacers of the first and second transistors or of the first transistor only; and

after forming the main spacers, performing a source/drain (S/D) implant to form a highly doped region within each of the DDD drain and source regions and the LDD drain and source regions, the highly doped regions being of the same conductivity type as and having a doping concentration greater than the DDD and LDD regions.

11. (original): The method of claim 10 wherein,

the extent of an overlap between the gate electrode of the second transistor and each of the LDD source and LDD drain regions is inversely dependent on a thickness of the off-set spacers,

a distance between an outer edge of each of the DDD source and DDD drain regions and an outer edge of the highly doped region within each of the DDD source and DDD drain regions is directly dependent on a combined thickness of the off-set and main spacers or on a thickness of the off-set spacer only, and

a distance between an outer edge of each of the LDD source and LDD drain regions and an outer edge of the highly doped region within each of the LDD source and LDD drain regions is directly dependent on a thickness of the main spacers.

12. (currently amended): The method of claim ~~1~~ 9 wherein the off-set spacers are from oxide or oxynitride.

13. (currently amended): ~~The method of claim 1 wherein,~~ A method of forming a MOS transistor, comprising:

forming a gate electrode over but insulated from a semiconductor body region;

~~said off-set spacers forming act further comprises~~ forming a layer of insulating material over the gate electrode including the side-walls of the gate electrode, and over exposed areas of the body region; ~~and~~

forming side-wall spacers along side-walls of the gate electrode over the layer of insulating material;

after forming the spacers, ~~said source and drain regions forming act further comprises~~ implanting impurities through the layer of insulating material to form ~~said~~ source and drain regions in the body region; and

removing a substantial portion of those portions of the insulting layer extending over the source and drain regions.

14. (currently amended): ~~The method of claim 1 wherein the off-set spacers forming act further comprises~~ A method of forming a semiconductor transistor, comprising:

forming a gate electrode over but insulated from a semiconductor body region;

forming a first layer of insulating material over the gate electrode and the body region;

forming a second layer of insulating material different from the first layer of insulating material over the first layer of insulating material; ~~and~~

etching ~~at least one of the first and~~ only the second layers of insulating material to form ~~the off set~~ spacers along the side-walls of the gate electrode;

implanting impurities through the first layer of insulating material to form a source region and a drain region in the body region; and

removing a substantial portion of those portions of the first layer of insulting material extending over the source and drain regions.

15. (canceled)

16. (currently amended): The method of claim 14 wherein the first layer of insulating material is oxide and the second layer of insulating material is nitride~~, the etching act further comprising:~~

~~etching only the nitride layer so that oxide-nitride off-set spacers are formed along the side-walls of the gate electrode while only the nitride is removed from all other areas~~.

17. (canceled)

18. (currently amended): The method of claim ~~1~~ 9 wherein thicker off-set spacers result in smaller overlap between the gate electrode and each of the source and drain regions.

19-76. (previously canceled)

77-89. (previously withdrawn)

90-99. (previously canceled)